Structural and electrical properties of metal-ferroelectric-insulator–semiconductor transistors using a Pt/Bi$_{3.25}$Nd$_{0.75}$Ti$_3$O$_{12}$/Y$_2$O$_3$/Si structure

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Abstract

The metal-ferroelectric-insulator–semiconductor (MFIS) capacitors were fabricated using the Pt/Bi$_{3.25}$Nd$_{0.75}$Ti$_3$O$_{12}$/Y$_2$O$_3$/Si(100) structure, yttrium sesquioxide (Y$_2$O$_3$) thin films as an insulating buffer layer with different thickness ranging from 10 to 40 nm were deposited on p-type Si(100) at room temperature by electron-beam evaporation method. Nd-modified bismuth titanate (Bi$_{3.25}$Nd$_{0.75}$Ti$_3$O$_{12}$:BNT) films were prepared as ferroelectric layers at a processing temperature of 750 °C by chemical solution deposition (CSD) method. The Y$_2$O$_3$ buffer layers show an amorphous structure, relatively high dielectric constant, and good electrical properties. The ferroelectric polarization–voltage (P–V) hysteresis was observed for Pt/BNT/Pt/Ti/SiO$_2$/Si and Pt/BNT/Y$_2$O$_3$/Si(100) capacitors. The MFIS structure exhibits a larger clockwise C–V memory window of 2.63 V when the thickness of Y$_2$O$_3$ layer was 10 nm and a lower leakage current density of 7·10$^{-9}$ A/cm$^2$ at a positive applied voltage of 6 V. Capacitance–voltage (C–V) and leakage–current density (J–V) characteristics of Pt/BNT/Y$_2$O$_3$/Si(100) capacitor indicate that the introduction of the Y$_2$O$_3$ buffer layer prevents the interfacial diffusion between BNT thin film and the Si substrate effectively and improves the interface quality. Furthermore, the Pt/BNT/Y$_2$O$_3$/Si structures exhibit excellent retention characteristics, the high and low capacitance values biased in the hysteresis loop are clearly distinguishable for over 13.6 days. The experimental results show that the BNT-based MFIS structure is suitable for non-volatile ferroelectric memory field-effect-transistors (FETs) with large memory window.

Keywords: MFIS; BNT; Y$_2$O$_3$; Memory window; Retention characteristic

1. Introduction

The ferroelectric memory is an ideal memory with clear advantages such as non-volatility, low power consumption, high endurance and high speed writing. This memory may be classified as two types. One is the capacitor type ferroelectric memory where the capacitor is the storage element and another is single transistor type ferroelectric memory where the storage element is the ferroelectric gate of the transistor. Among them, a ferroelectric gate field effect transistor (FET)-type memory is recognized to be excellent due to its nondestructive readout capability and compliance with the scaling rule, compared to the storage-capacitor type. The main challenge in realizing a FET-type...
memory is to obtain a reliable ferroelectric/Si interface because the interface diffusion and reaction increase the interface trap density and degrade the memory characteristics seriously [1,2]. To solve these problems, a buffer layer is usually inserted between ferroelectric layer and silicon substrate, forming a meta-ferroelectric-insulator–semiconductor (MFIS) structure [3]. Typical buffer-layer materials are HfO$_2$ [1], Y$_2$O$_3$ [4], CeO$_2$ [5], Si$_3$N$_4$ [6] and Al$_2$O$_3$ [7] which have relative high dielectric constants, low leakage current, good interface characteristics, and compatibility. Among them, the Y$_2$O$_3$ film has been well known to improve electrical characteristics of ferroelectric memory such as leakage current, memory window, and retention [8–10]. Various ferroelectric thin films such as SrBi$_2$Ta$_2$O$_9$ (SBT), PbZr$_x$Ti$_{1-x}$O$_3$ (PZT), and YMnO$_3$ have been used as ferroelectric gate materials in MFIS structures, in this paper, BNT is used for its larger $P_r$ and superior fatigue-free property [11,12].

In this work, the Y$_2$O$_3$ and BNT films were fabricated by electron-beam evaporation and CSD method, respectively. In order to show that the BNT-based MFIS structure is suitable for non-volatile memory FETs with large memory window, the electrical and structural properties of the MFIS structure at a relatively low processing temperature of 750 °C were investigated and evaluated by varying the Y$_2$O$_3$ layer thickness.

2. Experiment

3° p-type Si (100) wafers with resistivity 0.1 Ω·cm were used as substrates, which were cleaned by RCA to eliminate the native surface oxide layers. Then they were loaded into a vacuum chamber with a base pressure lower than 10$^{-9}$ Torr. Y$_2$O$_3$ films were deposited on wafers by evaporating Y$_2$O$_3$ ceramics tablets using an electron-beam gun. During deposition processing, the substrate temperature and chamber pressure were kept at room temperature and lower than 10$^{-7}$ Torr, respectively. The growth rate was about 1 nm/min. The thickness of Y$_2$O$_3$ thin films was in situ monitored with MDC-360 and adjusted in a range from 10 to 40 nm. After deposition, the samples were annealed at 800 °C for 30 min in oxygen ambient.

BNT films were deposited on the Y$_2$O$_3$/Si structure using CSD spin-coating method [13,14] at room temperature, dried at 400 °C for 10 min by rapid thermal annealing (RTA) in air to remove organic materials. Then, the films were annealed for crystallization in oxygen atmosphere at 750 °C for 1 h. The final thickness of BNT film was about 300 nm. In order to measure the electrical properties, dot-shaped Al and Pt top electrodes were deposited on Y$_2$O$_3$/Si and BNT/Y$_2$O$_3$/Si structures, respectively, at room temperature by vacuum evaporation through metal masks ($\phi = 0.2$ mm).

The structure and morphology of Y$_2$O$_3$/Si and BNT/Y$_2$O$_3$/Si were examined by X-ray diffraction (XRD) with Cu Kα radiation and atomic force microscopy (AFM). The surface roughness was recorded in 2.5 × 2.5 μm$^2$ by AFM. The characteristics of capacitance–voltage were measured using a HP4294 precision impedance analyzer by applying an a.c. signal of 50-mV amplitude and a dc bias voltage at 1 MHz frequency. The leakage–current characteristic was evaluated by a HP 4156 pA m/dc voltage source. The polarization–voltage ($P–V$) hysteresis loop was examined using a Ferroelectric Precision Workstation (Radiant Technologies Inc.) at room temperature.

3. Results and discussion

In order to improve the performance of the MFIS FET, one of the important points is that the Y$_2$O$_3$ buffer insulating layer should have small leakage current and a high dielectric constant. Fig. 1a shows a typical $C–V$ characteristics for an Al/Y$_2$O$_3$ (20 nm)/Si(100) capacitor measured at 1 MHz. The buffer layer of Y$_2$O$_3$ film was deposited at room temperature and subsequently annealed at 800 °C for 30 min. Well-behaved $C–V$ curve shows a negligible hysteresis loop (less than 6 mV) caused by charge-injection and ion-drift effects. The equivalent oxide thickness and the dielectric constant of the Y$_2$O$_3$ film calculated from the accumulation capacitance is about 4.75 nm and 16.03, respectively. Fig. 1b shows leakage current density versus voltage ($J–V$) characteristic for the same sample as that in Fig. 1a. The current density at 2.5 V is about 1.5 × 10$^{-7}$ A/cm$^2$, which indicates that the insulating property of the deposited Y$_2$O$_3$ film layer of MFIS structures is relatively good.

![Fig. 1. $C–V$ (a) and $J–V$ (b) characteristics for an Al/Y$_2$O$_3$/Si capacitor.](image-url)
Fig. 2 represents the XRD patterns of as-deposited Y₂O₃ (40 nm)/Si (a) and BNT/Y₂O₃/Si with various Y₂O₃ film thickness at 750 °C (b–e).

Fig. 2 shows the XRD patterns of BNT/Y₂O₃/Si at 750 °C and as-deposited Y₂O₃ (40 nm)/Si. As shown in Fig. 2, the Y₂O₃ film exhibits amorphous structure, no reflection peak is observed except the peak from the Si (200) plane. The film exhibits a very smooth surface morphology with a smaller root mean square (RMS) value of 0.7 nm. Usually, for MOSFET application, it is desirable to select a material that remains amorphous during the necessary processing treatments to reduce leakage currents, since grain boundaries may serve as high-leakage paths. Furthermore, grain size and orientation changes throughout a polycrystalline film can cause significant variation in dielectric constant, leading to non-reproducible properties [15]. XRD patterns for BNT/Y₂O₃/Si thin films with various Y₂O₃ film thickness annealed at 750 °C for 1 h are also displayed in Fig. 2. The bismuth layered perovskite structure appears with stronger peaks of (117), (006) and (001 2) without significant preferable orientation and secondary phases. The d values and intensities of the peaks in the XRD patterns are good consistent with those given in joint committee on Power Diffraction standards data card for Bi₄Ti₃O₁₂. The AFM image of BNT on Y₂O₃/Si shows smaller grains (45 nm) and a dense morphology with a smaller surface roughness of 4.8 nm.

Fig. 3 shows the corresponding P–V hysteresis loops of Pt/BNT/Pt/Ti/SiO₂/Si and Pt/BNT/Y₂O₃ (10 nm)/Si structures annealed at 750 °C. In Pt/BNT/Pt/Ti/SiO₂/Si structure, well-saturated P–V hysteresis loops are obtained, the remanent polarization (P_r) and coercive voltage (V_c) increase as the applied voltage increases from 2 to 5 V. The 2P_r value measured under a maximum applied voltage 5 V is about 28.5 μC/cm², this indicates that the BNT thin films with relatively good ferroelectric property have been fabricated in our present work. As to Pt/BNT/Y₂O₃/Si structure, usually real P–E hysteresis cannot be observed in MFIS capacitor because formation of depletion layer inhibits the polarization switching [16,17]. We have measured the P–V curves of all Pt/BNT/Y₂O₃/Si samples and found that evident non-saturating hysteresis loops with smaller remanent polarization are observed in Pt/BNT/Y₂O₃ (20 nm)/Si, Pt/BNT/Y₂O₃ (30 nm)/Si and Pt/BNT/Y₂O₃ (40 nm)/Si capacitors. This P–V behavior is ascribed to the fact that due to the applied voltage division between BNT and Y₂O₃ buffer layer, the voltage drop on the BNT layer is too small to cause polarization saturation. This type of P–V loop commonly occurs for metal-ferroelectric-semiconductor (MFS) and MFIS structures and is consistent with the theoretical prediction [18]. But interestingly, relatively saturated P–V hysteresis loop with a smaller remanent polarization (P_r) of 0.3 μC/cm² at an applied voltage of 5 V is observed in Pt/BNT/Y₂O₃ (10 nm)/Si capacitor, the corresponding memory window is 2.63 V. These non-saturating P–V curves were not shown in Fig. 3 b for clarity. The larger coercive voltage using Y₂O₃ film as insulating buffer layer lead to increase of the memory window, and then information storage capability improves.

The typical 1 MHz C–V characteristics of the Pt/BNT/Y₂O₃/Si capacitors with different thickness of Y₂O₃ thin films ranging from 10 to 40 nm are shown in Fig. 4. The thickness of BNT film is fixed at 300 nm. The insert displays the memory window of MFIS structure, measured at the corresponding thickness of the Y₂O₃ thin films, the memory window decreases from 2.63 to 1.1 V as the thickness of Y₂O₃ insulating buffer layer increases from 10 to 40 nm.
The applied voltage was swept at the speed of 0.1 V/s from −5 V to +5 V and from +5 V to −5 V. Theoretically, the memory window of the ferroelectric gate structure should be equal to twice of the coercive voltage, but the memory window is related to the mobile ions, coercive field, saturation level of the polarization, rearrangement of the space charge and interfacial polarization [17], and is also affected by the crystal orientation, film thickness and grain size of the ferroelectric thin film. In our C–V experimental results, the memory window of the Pt/BNT/Y2O3 (10 nm)/Si is 2.63 V, slightly smaller than that of the P–V hysteresis (2.68 V). The measured C–V characteristics exhibit clockwise hysteresis loops as expected for MFIS capacitor fabricated on a p-type semiconductor, as indicated by arrows, showing ferroelectric polarization switching type behavior. In order to check the effect of mobile ionic charges, interfacial polarization and rearrangement of the space charge on the hysteresis, the sweeping rate of the bias voltage was varied from 0.01 to 1 V/s. The memory window of Pt/BNT/Y2O3/Si annealed at 750 °C does not alter with the sweeping rate. This indicates that the hysteresis loop is caused due to ferroelectricity of the BNT films [1]. The ferroelectric border trap and mobile ion densities are much lower.

Leakage current density is an important consideration for device application. Fig. 5 exhibits the J–V characteristics of Pt/BNT/Y2O3/Si structure as a function of the Y2O3 layer thickness. As can be seen from Fig. 5, the leakage current densities are relatively low and the voltage dependence of the current densities is not strong. The leakage current density decreases as the thickness of Y2O3 insulating buffer layer increases from 10 to 40 nm. All leakage current densities are less than 7 × 10−9 A/cm² with a positive applied voltage up to 6 V, however, the leakage current densities with negative applied voltage are slightly larger than that of positive applied voltage due to a depletion layer is formed at the semiconductor surface when positive voltage is applied. This excellent result indicates that Pt/BNT/Y2O3/Si structures are suitable for MFIS non-volatile memory application especially for low voltage (<5 V), low power dissipation operation in the devices.

The retention characteristic is currently considered to be the most important issue for MFIS FETs application. Data retention periods from a few days to 30 days have been reported in MFIS FETs, as well as MFIS capacitors [1,19,20]. In this study, the C–t retention characteristics of the Pt/BNT/Y2O3/Si structures are illustrated in Fig. 6. In this measurement, after the “write” voltage pulses of ±5 V in height and 100 ms in width were applied to the samples, the time dependences of the high and low capacitance values were measured separately, keeping the bias voltage at 1.5 V. As can be seen from Fig. 6, the capacitance values are clearly distinguishable for over 13.6 days, which is much longer than 5 days reported by Park et al. [1]. Therefore, it is concluded that the Pt/BNT/Y2O3/Si structure is one of the most promising candidates for realizing FET-type ferroelectric random access memories with a long data retention time.

4. Conclusions

A Pt/BNT/Y2O3/Si(100) MFIS structure with different thickness of Y2O3 insulating buffer layer was successfully
fabricated by electron-beam evaporation and CSD method, respectively. The Y$_2$O$_3$ film exhibits amorphous structure and BNT film shows the typical XRD patterns of BTO layered perovskite polycrystalline structure. The MFIS structure exhibits a larger clockwise $C$–$V$ memory window of 2.63 V and a lower leakage–current density of $7 \times 10^{-9}$ A/cm$^2$ at a positive applied voltage of 6 V. The memory windows of the MFIS structure become larger with decreasing the Y$_2$O$_3$ thickness, moreover, they remain constant while the sweeping rate of the bias voltage and the measuring frequency are varied. This indicates that the hysteresis loop is caused by ferroelectricity. Meanwhile, the ferroelectric border trap and mobile ion densities are lower. Furthermore, the Pt/BNT/Y$_2$O$_3$/Si structures exhibit excellent retention characteristics, the high and low capacitance values biased in the hysteresis loop are clearly distinguishable for over 13.6 days. The experimental results can be concluded that the Pt/BNT/Y$_2$O$_3$/Si(100) MFIS structure is suitable for non-volatile memory FETs with large memory window in low voltage, low power dissipation operation.

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